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EXAMINER	
SILVER, DAVID	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,981	WASYNCZUK ET AL.	
	Examiner	Art Unit	
	David Silver	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *5* is/are withdrawn from consideration.

5)☒ Claim(s) *8-10* is/are allowed.

6)☒ Claim(s) *1-4,6,7,11-14 and 16* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 were originally presented for examination.

2. Claims 1-16 were rejected.

3. Claims 8-10 and 15 contained allowable subject matter.

4. Claims 5 were cancelled and therefore withdrawn from consideration.

5. Claims 1-4, 6-16 are currently pending in Instant Application.

6. The Instant Application is not currently in condition for allowance.

Response to Arguments

7. Applicant's arguments filed 2/16/06 have been fully considered but they are not persuasive for the reasons enumerated below.

Response: Objected to Claim

8. The Examiner thanks the Applicant for canceling claim 5 and thereby rendering the objection moot.

Response: 35 USC 112 second paragraph

9. The rejection of claim 8 with respect to lack of antecedent basis for the limitation "B^{CA}_{link}" has been withdrawn

10. The Examiner thanks the Applicants for clarifying the meaning and setting the metes and bounds of the phrase "negative of the minimum of all controlling elements". It will be interpreted as presented in Section C of Response to Office Action **("ROA")** dated 2/16/06. The 35 USC 112 second paragraph rejection of claim 15 has been withdrawn.

Response: 35 USC 101

11. The Examiner thanks the Applicants for complying with 35 USC 101. The rejection 35 USC 101 rejection of claims 8-10 has been withdrawn.

Response: 35 USC 102(b) Rejection

12. **As per claim 1,**

Applicants argue primarily that:

"... the present invention as claimed in claim 1 utilizes a computer [to] develop and solve state equations of the form

$dx/dt = f(x,t)$; $x(0) = x_0$
Given a state model, the transient response can be solved using any suitable state equation solver. The cited TINA software does not use this methodology."

Examiner Response:

It is noted that the Applicants have argued that the prior-art does not disclose a solving first-order ordinary differential state equation in the form of: $dx/dt = f(x,t)$; $x(0) = x0$. It is noted that Applicants have limited state equations to first order.

However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., generated a state equation of the form $dx/dt = f(x,t)$; $x(0) = x_0$) are not recited in the rejected claim 1. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The Examiner has respectfully traversed this argument.

As per claims 2-4, 6-7, 16, and 12-14,

Applicants have provided no specific arguments for claims **2-4, 6-7, 16, and 12-14**. The Examiner therefore maintains the rejection of the claims **2-4, 6-7, 16, and 12-14**.

Claim Interpretation

It is noted that the Applicants have limited the claimed state equation to a first-order ordinary differential equation in the form of: $dx/dt = f(x,t)$; $x(0) = x0$. **(Remarks in Response to Office action Middle of page 14)**

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

MPEP 2131.01 Multiple Reference 35 U.S.C. 102 Rejections recites
"Normally, only one reference should be used in making a rejection under 35 U.S.C. 102. However, a 35 U.S.C. 102 rejection over multiple references has been held to be proper when the extra references are cited to: (A) Prove the

primary reference contains an "enabled disclosure;" (B) Explain the meaning of a term used in the primary reference; or (C) **Show that a characteristic not disclosed in the reference is inherent."**

13. Claims 1-4, 6-7, 11, and 16 rejected under 35 U.S.C. 102(b) as being anticipated by TINA Pro.

As per claim 1, the reference implements a method, comprising:

creating one or more data structures sufficient to model an electronic circuit as a collection of n elements consisting of:

zero or more LRV elements, each having at least one of

(a) a non-zero inductance parameter L_{br}, (b) a non-zero resistance parameter r_{br}, or (c) a non-zero voltage source parameter e_{br},**("Electronic Components in TINA" hereinafter referred to as "ECTINA": Passive Components: Inductor, Resistor, Sources: Voltage Source. Example of said modeling can be seen in the image on page "Symbolic Circuit Analysis")**, but

neither a non-zero capacitance parameter, nor a non-zero current source parameter, nor a switch parameter **(ECTINA: Passive Components: Capacitor, Sources: Current Source, Other: voltage controlled switch)**;

zero or more CRI elements, each having at least one of

(a) a non-zero capacitance parameter C_{br}, (b) a non-zero resistance parameter r_{br}, or (c) a non-zero current source parameter j_{br},**(ECTINA: Passive Components: Capacitor, Resistor, Sources: Current Source)**, but

neither a non-zero inductance parameter, nor a non-zero voltage source parameter, nor a switch parameter **(ECTINA: Passive Components: Inductor, Sources: Voltage Source, Other: voltage controlled switch)**;

and zero or more switching elements, each having a switch state **(ECTINA: Other Components: time controlled switch, voltage controlled switch, Flip-flops)** and neither a non-zero inductance parameter, a non-zero capacitance parameter, a non-zero resistance parameter, a non-zero voltage source parameter, nor a non-zero current source

parameter **(See Examiner notes below on component characteristics and modification)**;

and automatically generating a first set of state equations from said one or more data structures **("Symbolic Circuit Analysis" hereinafter referred to as "SCATINA" lines 1-2)**;

and simulating operation of the electronic circuit by application of said first set of state equations;

wherein n is at least two, and the collection comprises either

an LRV element for which at least two of L_{br}, r_{br}, or e.sub.br are non-zero, or a CRI element for which at least two of C_{br}, r_{br}, or j_{br} are non-zero **(See Examiner note and assertion 1 below)**.

Note: The components of TINA Pro can work in either ideal mode where all characteristics are set to zero, or the user is able to specify which parameters to add to the simulation (i.e., a voltage sources having associated resistance) (ECTINA, line 1-2 "which can be modified by the user").

Assertion 1: The Examiner also asserts the creation of the mentioned circuit can be manually done by the user. As such, the parameters can be entered by the user. Additionally, the user can place as many components into the computer aided design program as he or she wishes, which includes 2 or more of the above-mentioned components.

As per claim 2, the reference implements a method of claim 1, wherein said simulating comprises

producing state output, data, the method further comprising **("Circuit Simulation" hereinafter referred to as "CSTINA" lines 1-2 and figure)**:

modifying the parameters in said first set of state equations as a function of said state output data **(ECTINA, Flip-flops, See assertion below)**.

As per claim 3, the reference implements a method of claim 1, further comprising:

modifying the parameters in said first set of state equations based on a time-varying parameter of at least one element in said collection **(ECTINA: Other components: time controlled switch)**.

As per claim 4, the reference implements a method of claim 1, further comprising:

generating a second set of state equations from said one or more data structures upon the occurrence of a first topology change event **(ECTINA: Other components: time controlled switch)**.

As per claim 6, the reference implements a method of claim 4, wherein each unique vector of switch states represents a topology of the overall circuit, and further comprising:

storing said first set of state equations in a cache; after a second topology change event, determining whether a set of state equations in the cache represents the new topology; if said determining is answered in the affirmative, using the set of state equations that represents the new topology to simulate operation of the circuit after the second topology change event; and if said determining is answered in the negative, building a third set of state equations that represents the new topology, **and** using the third set of state equations to simulate operation of the circuit after the second topology change event **("TINA: Toolkit for Interactive Network Analysis" hereinafter referred to as "Frontpage", lines 1-2)**.

As per claim 7, the reference implements a method of claim 6, further comprising:

storing said second set of state equations in a cache; after a third topology change event, deciding whether a set of state equations in the cache represents the new topology; if said deciding is concluded in the affirmative, using the set of state equations from the cache that represents the new topology to simulate operation of the circuit after the third topology change event; and if said deciding is concluded in the negative, building a new set of state equations that represents the new topology, and using the new set of state equations to simulate operation of the circuit after the third topology change event **("TINA: Toolkit for Interactive Network Analysis" hereinafter referred to as "Frontpage", lines 1-2)**.

This claim is rejected under same assertion as claim 6.

As per claim 11, the reference implements a system, comprising

a processor and a computer-readable medium in communication with said processor

(Frontpage, "The Complete Electronics Lab for Windows" TINA is an application

designed to run on Windows, as such it inherently requires a processor and memory in communication with the processor),

said medium containing programming instructions executable by said processor to:

build state equations for a first topology of an electronic circuit having at least two switching elements, wherein each switching element has a switching state **(ECTINA time controlled switch. It is inherent that TINA has instructions to be executed by the processor to add components including, but not limiting to time an voltage controlled switching elements.)**

solve said state equations at time t_i to provide a state output vector, in which at least two elements control the switching states of the switching elements **(CSTINA: The image shows an output vector (graph) as a time t_i, displayed on the x-axis. The output vector can be referring to the output of the said equations on a graph at a particular time. Therefore, at time 0, the output vector is <collector, base> is <13mV, 2mV> and at time 100mS it is <-5mV, 0mV> as shown in the figure displayed on page CSTINA);**

calculate the value of a switching variable as a function of the state output vector, wherein the value reflects whether the switching state of at least one of the switching elements is changing **(ECTINA: Flip-flop, See Examiner assertions below)**;

and if the value of the switching variable at time t_i indicates that at least one of the switching elements is changing, determine a second topology of the electronic circuit for time t_i^+ and obtain state equations for the second topology **(ECTINA: Other components: time controlled switch, See Examiner assertion 1)**.

Assertion 1: The Examiner asserts that it is inherent that TINA generates a new equation upon a topological change, such as that of a switch change, in order to continue producing valid results within accordance of the new circuit configuration.

Assertion 2: The Examiner asserts that in order for D flip-flop simulation to occur the simulator inherently uses the output of the flip-flop to feedback into the input of the flip-flop (in case of a

feedback loop) and as such the simulator modified the parameters of the said first equation as a function of the output.

Assertion 3: The Examiner asserts that the switching variable can be merely a Boolean function wherein if one switch is changing its value the Boolean will be, for example, "true" to reflect that a change has occurred, and "false" if no change has occurred.

As per claim 16, the reference implements a system for simulating electronic circuits, comprising a processor and a computer-readable medium in communication with said processor, said medium containing programming instructions executable by said processor to read element parameters and node connection information from a data stream comprising at least one switch type specification, the at least one switch type specification being selected from the group consisting of:

a unidirectional, unlatched switch ;a bidirectional, unlatched switch; a unidirectional, latched switch; and a bidirectional, latched switch **(ECTINA: Flip-flops: D latch)**;

and wherein said instructions are further executable by said processor automatically to calculate state equations for the circuit given the states of switches specified by said at least one switch type specification **(SCATINA lines 1-2 and displayed image. It is inherent that instructions are executed by the said processor to calculate the state equation for the given switches)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over TINA as applied to claim 11 above, and further in view of MathWorks (http://web.archive.org/web/20010309234347/http://web.ccr.jussieu.fr/ccr/Documentation/Calcul/matlab5v11/docs/00000/0007e.htm, 1997) (hereinafter "MathWorks") (See PTO-892 for reference information).

As per claim 12, TINA teaches of system which includes instructions to solve and build state equations and resolve switching logic. As such it must have block of code (modules) to accomplish the mentioned tasks. TINA does not however explicitly disclose using an ordinary differential equation solver module. However, MathWorks teaches of an exemplary analogous simulation system using such ODE solvers, as stated on page "SIMULINK 2; Simulation Engine" section "New ODE Solvers". It is inherent that such a system which includes an ODE solver. Additionally, it is inherent that the building, solving, and determining are performed by their respective modules.

It would have been obvious to one of ordinary skill in the art of simulation, at the time of the present invention, to combine the teachings and implementations of the references. In fact, motivation to combine would have been to create a faster and more powerful circuit simulation engine and, for example, to include non-linear components such as transistors and RLC circuits.

As per claim 13, the reference discloses a system of claim 12, wherein said obtaining is performed by said switching logic module **(ECTINA: Other: time/voltage controlled switch)**. The Examiner asserts that it is inherent that TINA uses at least switching logic code (module), and likely other modules, in order to simulate a circuit containing one or more switching components such as the ones referenced above.

As per claim 14, the reference discloses a system of claim 12, wherein said obtaining is performed by said state equation building module **(ECTINA: Other: time/voltage controlled switch)**. The Examiner asserts that it is inherent for TINA to use at least state equation building code (module), and likely other modules, in order to display the circuit equation as shown in webpage SCATINA image titled "bandpass".

Allowable Subject Matter

15. The following is the Examiner's statement of reasons for allowability:

16. As per claim 8-10, the instant claim is directed to a non-obvious improvement over the computer application as implemented in TINA Pro.

The most relevant prior-art of record is TINA Pro that discloses the claim as follows **(particularly note the emphasizing portion)**:

It discloses the calculation of inductive branches, capacitive brunches and resistance branches.

However, the prior art does not explicitly disclose or suggest: creating one or more data structures that together store characteristics of a plurality of active branches B^{active} that make up a graph of nodes and branches that form a circuit, wherein B^{active} consists of a set B_L of zero or more inductive branches, each having a non-zero inductive component but neither a capacitive component nor a variable switch state; a set B^C of zero or more capacitive branches, each having a non-zero capacitive component but neither an inductive component nor a variable switch state; and a set B^A of additional branches, each having neither an inductive component, nor a capacitive component; partitioning B^{active} into a first branch set B.sub.tree.sup.active and a second branch set B.sub.link.sup.active, where the branches in B.sub.tree.sup.active form a spanning tree over B^{active}, giving priority in said partitioning to branches not in B^L over branches in B.sup.L; sub-partitioning B.sub.link.sup.active into a third branch set B.sub.link.sup.L and a fourth branch set B.sub.link.sup.CA, where B.sub.link.sup.L=B.sub.link.sup.active.andgate.B.sup.L; identifying a fifth branch set B.sup.CA as the union of B.sub.link.sup.CA, B.sup.C.andgate.B.sub.tree.sup.active, and those branches in B.sub.tree.sup.active that form a closed graph when combined with B.sub.link.sup.CA; partitioning B.sup.CA into a sixth branch set {tilde over (B)}.sub.tree.sup.CA and a seventh branch set {tilde over (B)}.sub.link.sup.CA, where the branches in {tilde over (B)}.sub.tree.sup.CA form a spanning tree over B^{CA}, giving priority in said partitioning to branches in B^C over branches not in B^C; identifying an eighth branch set B.sub.tree.sup.C={tilde over (B)}.sub.tree.sup.CA.andgate.B.sup.C; selecting a set of state variables comprising: for each branch of B.sub.link.sup.L, either the inductor current or inductor flux, and

for each branch of B.sub.tree.sup.C, either the capacitor voltage or capacitor charge; and simulating a plurality of states of the circuit using the set of state variables.

17. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
18. As per claim 15, the instant claim is directed to a non-obvious improvement over the computer application as implemented in TINA Pro.

The most relevant prior-art of record is TINA Pro in view of further in view of MathWorks **(http://web.archive.org/web/20010309234347/http://web.ccr.jussieu.fr/ccr/Documentation/Calcul/matlab5v11/docs/00000/0007e.htm, 1997)** that discloses the claim as follows:

TINA Pro discloses a processor and a computer-readable medium in communication with said processor **(Frontpage)**,

said medium containing programming instructions executable by said processor to:

build state equations for a first topology of an electronic circuit having at least two switching elements, wherein each switching element has a switching state **(ECTINA time controlled switch)**

solve said state equations at time t_i to provide a state output vector, in which at least two elements control the switching states of the switching elements **(CSTINA: The image shows an output vector (graph) as a time t_i, displayed on the x-axis);**

calculate the value of a switching variable as a function of the state output vector, wherein the value reflects whether the switching state of at least one of the switching elements is changing **(ECTINA: Flip-flop)**;

and if the value of the switching variable at time t_i indicates that at least one of the switching elements is changing, determine a second topology of the electronic circuit for time t_i^+ and obtain

state equations for the second topology **(ECTINA: Other components: time controlled switch)**.

MathWorks teaches of an exemplary analogous simulation system using such ODE solvers, as stated on page "SIMULINK 2; Simulation Engine" section "New ODE Solvers".

However, TINA Pro and MathWorks do not individually or in combination, teach, suggest, or render obvious that at a time t.sub.j, at least two switching elements are each either rising-sensitive or falling-sensitive switches, wherein rising-sensitive switches change switching state if and only if a controlling element of the state vector has passed from a negative value to a non-negative value; and falling-sensitive switches change switching state if and only if a controlling element of the state vector has passed from a positive value to a non-positive value; and the function is the arithmetic maximum of a maximum of all elements of the state vector that control rising-sensitive switches, and the negative of the minimum of all controlling elements of the state vector that control falling-sensitive switches.

19. These limitations in context of the claim as defined in the specification and by claim interpretation are not taught and suggested by prior art of record.
20. The art of record, either individually or in combination, fails to teach, suggest, or render obvious invention having the corresponding function that is claimed. In view of the foregoing, the Instant Claims of the present application are found to be patentable over the prior art.

Conclusion

21. Claims 1-4, 6-7, 11-14 and 16, are rejected.
22. Claims 8-10 are allowable.
23. Claim 15 is objected to.
24. The Instant Application is not currently in condition for allowance.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Silver
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/ds/
4/13/06